Quasi 3D simulation of Super Junction IGBT, 1200V class.

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Abstract

We report the simulation results 1200V Super Junction (SJ) IGBT, and discuss the Quasi 3D simulation limitation.

The SJ IGBT demonstrated results shows remarkable trade-off performance Eoff vs. Vce(sat) and has high latch-up immunity. Simulated structure is fully manufacturable, short circuit ruggedness and hot leakage current were taken into account.

I. Introduction

The main development trend for power semiconductor devices has a target increasing power density for a given application. In recent years there are many research reports of the SJ power devices, which is the charge compensation devices with low on-resistance below the so called theoretical Si limit [1].

SJ devices have a drift region arranged as pillars of high doping concentration p and n-types. Such structure is charge balanced, i.e. donors and acceptors net charge is equal to zero. Such idea returning us to the ideal power switch concept: dielectric behaviour at off-state and high conductivity at on-state. Similarity to dielectric originated from flat field strength E value along the SJ layer.

SJ structures fabrication is still remain a technology challenge [2]. Technology deviations for zero net charge condition is allowed not more than ±10%. Also high breakdown voltage demands small cell pitch size with combination a wide SJ area. It leads us to high aspect ratio for SJ cell design.

Two main fabrication technologies are using for SJ devices: refill trench and multi epi step [3,4]. Both technologies are still competitive due to high charge imbalance sensitivity of SJ structure. SJ area topology also can differ, it can be arranged as stripes or pillars.

SJ MOSFETs [5,6] are industrially manufacturing devises now. Recently, several publications were issuing SJ bipolar device [7-9]. The reason switch to bipolar technology is obvious: use both carrier types instead one at SJ MOSFET and thus increase power density for a given device area. Increasing power density leads to problems with device control. Additionally, SJ structure for IGBT provide more latch-up immunity because of higher n-drigt doping density. Research how to keep full controllability over device with higher energy density is the subject for this paper.

In this paper we issuing Quasi 3D simulation of Super Junction IGBT, multi epi step technology and pillar structure. Simulated structure is fully manufacturable. Important for real application parameters are discussing: saturation current Isat and saturation voltage Vce(sat).

II. Device structure

It is two main SJ structures manufacturing technology exists: trench refill and subsequent boron implantation and epi growth steps. For implantation technology long drive-in is needed in order to merge p-implanted regions. For such technology step epi thickness is limited by cell size because lateral p-pillar diffusion should left enough space for n-pillars, otherwise structure resistance can be high.

For SJ layout also two main ways exists: stripes and pillars structures.

All mentioned structures have to provide net charge balance in order to achieve maximum breakdown voltage. Due to SJ structures similarity field strength distribution to dielectrics, maximum BV is given by simple formula:

$$BV=Ecrit*tsj$$

Where critical field Ecrit ~2.5E5 V/cm, tsj – super junction structure thickness.

In lateral direction limitation factor also exist. With applying voltage to anode electrode SJ structure starts depleted laterally first. In such case maximum BV condition is follow: SJ structure has to be fully depleted laterally before field strength achieve Ecrit. It gives relation between cell doping charge and size, which depends from technology and layout. In Table 1 shown maximum drift layer doping Nd for different structures types.

Table 1.

Layout and technology.	**Maximum epi doping Nd.**
Implanted Stripe.	$N_d \leq E_{crit} \cdot \varepsilon_{si}/q \cdot C_p$
Refilled trench, Stripe.	$N_d \leq 2 \cdot E_{crit} \cdot \varepsilon_{si}/q \cdot C_p$
Implanted pillar	$N_d \leq 2 \cdot E_{crit} \cdot \varepsilon_{si}/q \cdot C_p$
Refilled pillar	$N_d \leq 8 \cdot E_{crit} \cdot \varepsilon_{si}/q \cdot C_p$

Where N_d – donor doping density, C_p – cell pitch.

Trenched structures can be simulated with 2D cells good enough. For the pillar structure quasi-3D simulation, i.e cylindrical symmetry cell is more appropriate.

Fig. 1. shows the 1.2 kV simulated device structure. Structure parameters shown at Table 2. MOS P- region doping was fitted to provide threshold voltage Vth=5 V @ Jc=1E-2 A/cm^2, channel length is about 1 um.

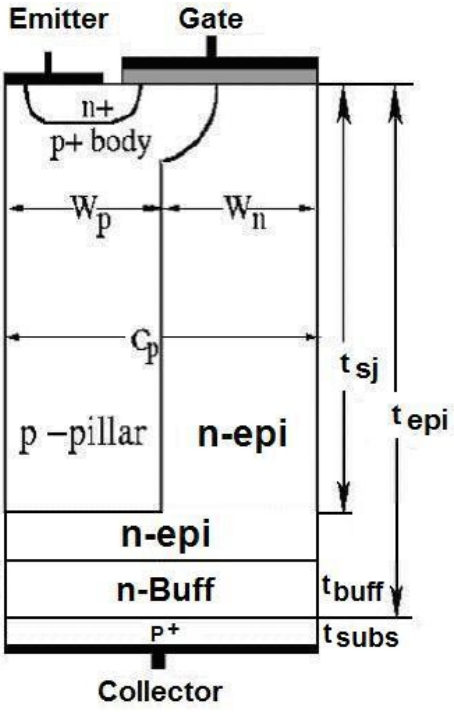

Fig.1. Simulated structure.

Table 2.

Structure parameters	Value
Cp	6.7 um
Wp	3.5 um
tsj	72 um
tbuff	20 um
tepi	100 um
tsubs	10um

Nd Epi	1E14-3E15 cm^-3
Na pillar	3.66E14- 1.1E16cm^-3
N-Buffer conc	3E17-1.3E18 cm^-3
Substrate resistance	RHO=0.06 Ohm*cm
Temperature (if not specified)	T=25 C
Carrier lifetime	2 - 10 us

III. Simulation results.

A. Off-state characteristics.

SJ structure doping variations have a big influence to breakdown voltage. Charge imbalance can be defined as

$$CB=(Qp-Qn)/Q0,$$

Where Qp – holes charge, Qn- electrons charge, Q0 – balanced charge, it is equal Qp or Qn at Qp=Qn. Breakdown voltage dependence from charge imbalance shown at Fig.2. Curves maximum shift regarding CB=0 is due to coarse simulation grid.

Window of existence for desired BV=1.2 kV is depending from epi layer doping and gets wider at low doping concentration. However low epi concentrations increases structure resistance, therefore epi concentration should be selected as high as it allowed by technology variations. For the Nd=1E15 cm^-3 curve width at BV=1.2 kV is ±8.5%, it is enough for good production yield. For the following simulations Nd= 1E15 cm^-3.

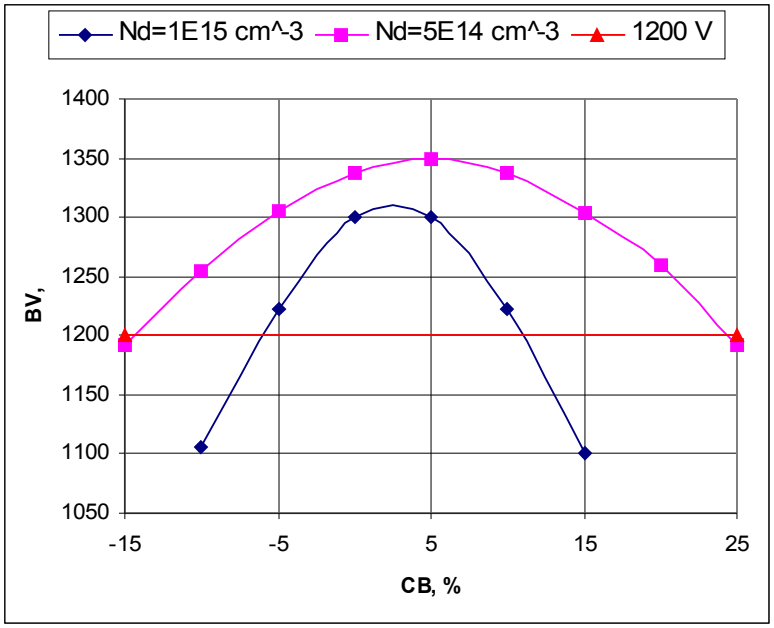

Fig.2. Breakdown voltage regarding SJ region charge imbalance.

Preventing thermal run during off-state at temperature T=125 C is very important from practical point of view. Such targeting leads to suppressing the hot leakage current density Jces(hot). Optimising the n-buffer doping density could reduce this current. Further simulations were performed to optimise n-buffer doping density in order to suppress Jces(hot). As Jces(hot) limitation factor n-buffer doping was used, i.e. collector efficiency control.

Fig. 3 shows the dependence of the collector emitter saturation voltage Vce(sat) and a hot leakage current Jces(hot) on the density ratio GAMMA of the densities of the p+ collector and

n-buffer layer (=C(p+)/C(n)). The result was the ability to reduce Jces(hot) while avoiding any increases in Vce(sat).

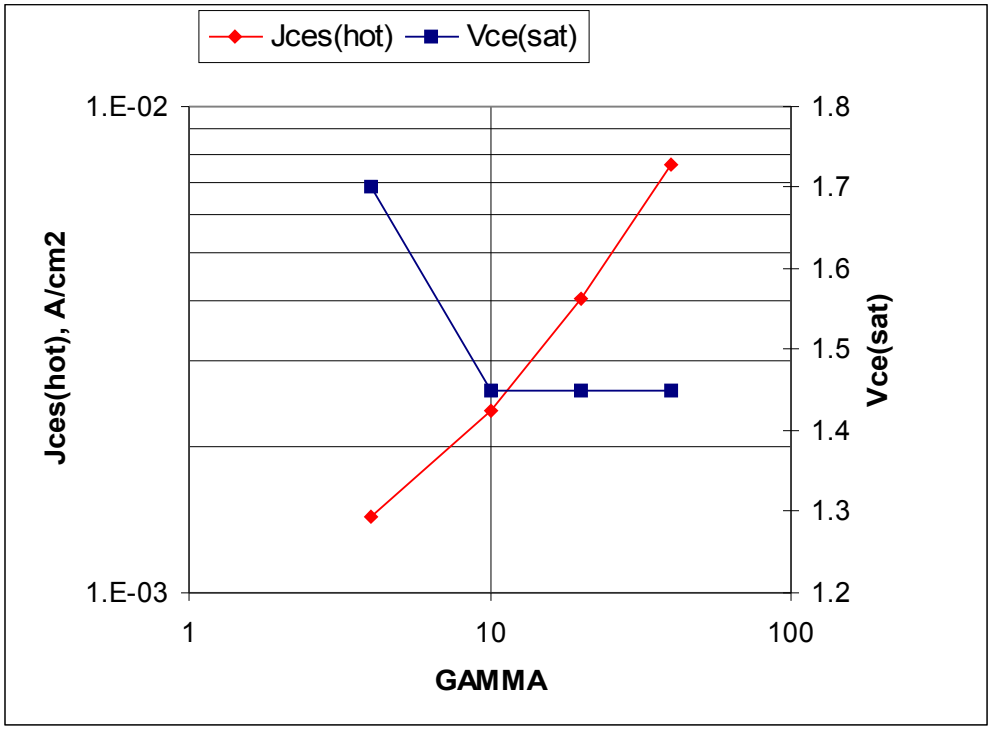

Fig.3. Dependence Vce(sat) and Jces(hot) on GAMMA at T=125 C.

B. On-state characteristics.

The super junction structure makes up an unique plasma distribution across the device. In the SJ IGBT electron-hole plasma originating at the collector. Emitter side plasma tend to segregate and unipolar current flows in p and n pillars. Compared to conventional IGBTs that gives lower Vce(sat) at same current density.

Saturation current density Isat appears to be very high at gate voltage Vge=15V for devices with threshold voltage Vth ~5 V (Fig.4). It leads to short circuit test failure. In order to reduce Isat three possible solutions are possible:

i. Vth increasing

ii. Operating at low gate voltage range Vge~8-10 V.

iii. Decreasing MOSFET channel density, i.e. replace “active” p-pillars with “idle” ones, without MOSFET transistor.

For further simulations decreased Vge=8 V voltage was used.

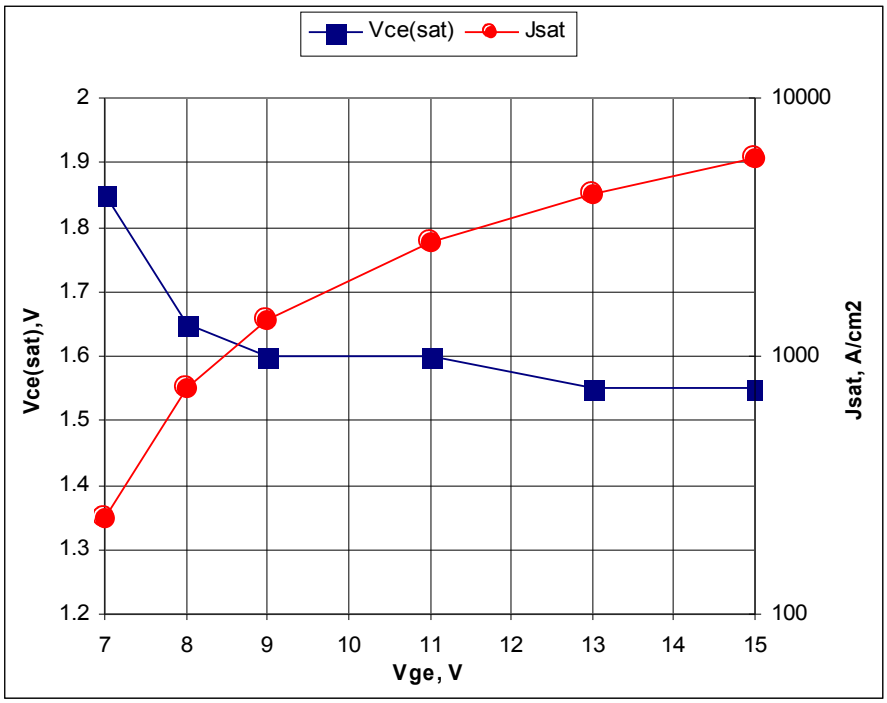

Fig.4.Vce(sat) and Jsat vs. Vge

IV. Switching losses.

Because of plasma distribution dependence from epi doping (i.e. p-pillar doping) optimisation for SJ IGBT switching performance is needed. Fig. 5 shows Eoff and Vce(sat) dependence from epi doping. Both values are decreasing while doping concentration rising. Limitation factor is p-pillar doping technology variation which reducing breakdown voltage curve width. Switching simulations were performed with resistive load, Vce=600 V, Jc=100 A/cm2

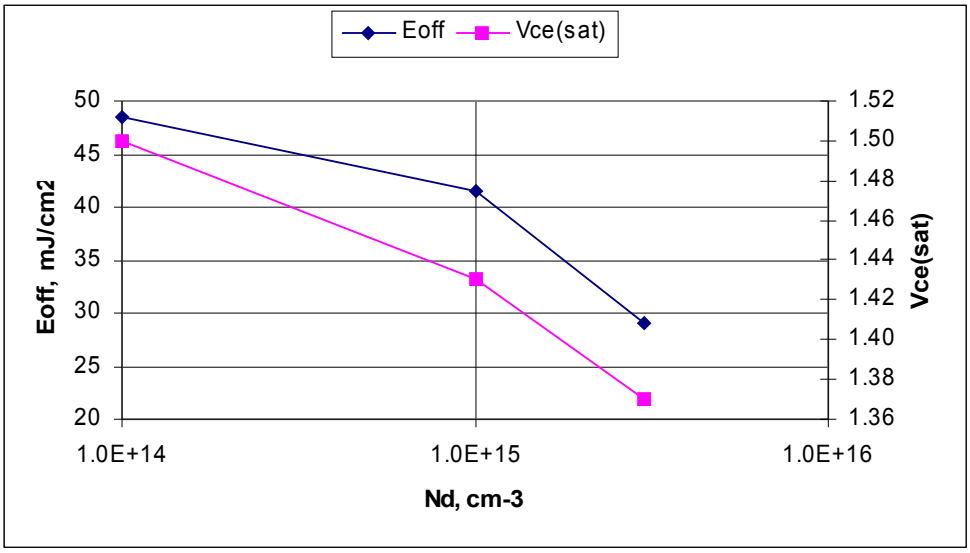

Fig.5 Eoff and Vce(sat)

Simulated trade-off curves are shown at Fig. 6. These curves demonstrates normalized switching losses Eoff per Ampere and conduction losses at reasonable current density.

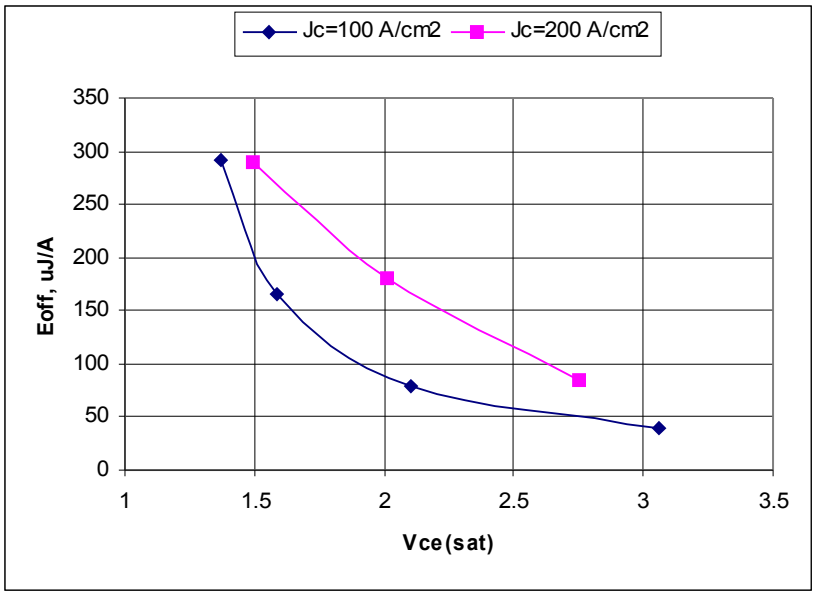

Fig. 6. Trade-off curve

IV. Discussion.

Simulated SJ IGBT structure has design with technology restrictions: cell pitch Cp=6.7 um (or distance between centres neighbour p-pillars is 13.4 um), super junction region depth is 72 um. It should be mentioned longer p-pillar is more effective in eliminating the stored hole charge, leading to fast switch-off time. But increasing p-pillar depth leading to increasing number of subsequent epi end boron implantation steps. Currently structure suppose to manufacture with 8 epitaxial growth, 9 um each layer.

Another limitation for selected technology is n-drift region partial compensation with diffused boron. This effect requires additional research.

V. Conclusions.

Trough quasi-3D simulation study, fully manufacturable SJ IGBT has been verified. SJ IGBT shows remarkable trade-off performance for Vce(sat) and Eoff because of unique plasma distribution in the device.

Practical IGBT restrictions such as: short circuit current, hot leakage current and breakdown voltage with technology deviations were considered. Practical steps for eliminating negative effects were suggested.

Switching IGBT technology to super junction leads to radical changes in device performance. SJ based IGBT will be next generation IGBT technology

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